



combinational (gate OR logic) static timing analysis

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G Yee, C Sechen - Computer Design: VLSI in Computers and Processors, 1996. ...  
 1996 - [ieeexplore.ieee.org](#)

... logic gates by simply replacing the static gate library with a CD domino gate library ...

Once a combinational logic netlist has been generated, CDLD's have ...

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**Timing optimization of combinational logic**

KJ Singh, AR Wang, RK Brayton, A Sangiovanni-Vincentelli - Computer-Aided Design, 1988.  
 ICCAD-88. Digest of Technical Papers, 1988 - [ieeexplore.ieee.org](#)

... Vimiceimtelhi Timing Optimization of Combinational Logic \* CH2657-5 ... in whelm a- conipex

gate is implemented ... literahs in the duplicated logic, VP1 = Potential ...

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**Timing verification of sequential domino circuits - group of 14 »**

D Van Campenhout, T Mudge, KA Sakallah - International Conference on Computer-Aided Design, 1996 - [doi.ieeeecomputersociety.org](#)

... ANDOR gate (whose output is s) switches. ... circuit implemented in a mix of static and

domino logic. ... a preprocessing step that computes the combinational delays. ...

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**Clock-delayed domino for dynamic circuit design - group of 5 »**

G Yee, C Sechen - Very Large Scale Integration (VLSI) Systems, IEEE ... , 2000 - [ieeexplore.ieee.org](#)

... Thus, combinational logic blocks can be designed having the ... standard cell library and dynamic gate netlist ... using static CMOS or standard domino logic, a common ...

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**A unified single-phase clocking scheme for VLSI systems - group of 3 »**

M Afghahi, C Svensson - Solid-State Circuits, IEEE Journal of, 1990 - [ieeexplore.ieee.org](#)

... on the minimum short-path delay of the combinational logic circuit ... To gate the clock signal with a data signal or to delay ... 3 this static ETDF is demonstrated ...

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**Wave-domino logic: timing analysis and applications**

W Lien, W Burleson - Circuits and Systems, 1992. ISCAS'92. Proceedings., 1992 ... , 1992 - [ieeexplore.ieee.org](#)

... We partition the original combinational circuit into n stages ... restructuring of a circuit to equalize logic structure and ... If we treat a gate like an information ...

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**Dynamic logic synthesis**

G Yee, C Sechen - Custom Integrated Circuits Conference, 1997., Proceedings of ... , 1997 - [ieeexplore.ieee.org](#)



combination static timing domino (reverse OR

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[N Vasseghi](#)

[Skew safety and logic flexibility in a true single phase clocked system](#)

P Larsson - Circuits and Systems, 1995. ISCAS'95., 1995 IEEE ... - [ieeexplore.ieee.org](#)

... A clock skew insensitive **combination** is shown in Fig. ... P latch + N latch is replaced by **static** logic followed ... We discuss **timing** of and logic placement in True ...

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[Harmony: \*\*static\*\* noise analysis of deep submicron digital integrated circuits - group of 9 »](#)

KL Shepard, V Narayanan, R Rose - Computer-Aided Design of Integrated Circuits and Systems, ..., 1999 - [ieeexplore.ieee.org](#)

... The global level involves a careful **combination** of **static** noise analysis ... ways, this graph is analogous to the **timing** graph used in **static timing** analysis. ...

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[Static timing analysis of irreversible crosstalk noise pulse faults - group of 4 »](#)

M Phadoongsidhi, KK Saluja - VLSI Design, 2004. Proceedings. 17th International ..., 2004 - [ieeexplore.ieee.org](#)

... not practical to consider every possible **combination** of nets ... We can describe a **static timing** analysis of the ... node and proceeds in **reverse**, iteratively updating ...

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[Method for performing transistor-level \*\*static timing\*\* analysis of a logic circuit - group of 3 »](#)

TM Burks, RE Mains - US Patent 5,946,475, 1999 - Google Patents

... 1, which shows a **domino** AND gate 100 designed to ... **combination** of input values accurately

reflects the operating ... 'transistor level **static timing** analysis approach ...

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[\[PDF\] Incorporating Signal Dependencies into \*\*Static\*\* Transistor-Level Delay Calculation](#)

TM Burks, RE Mains - TAU: ACM/IEEE International Workshop on Timing Issues in the ..., 1997 - [eecs.umich.edu](#)

... Many path-based **timing** ... This **combination** of input values accurately reflects the operating ... the next section, we describe a method for **static** delay calculation ...

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[Design scan test strategy for single phase dynamic circuits - group of 3 »](#)

CH Cheng - Defect and Fault Tolerance in VLSI Systems, 2003. ..., 2003 -

[ieeexplore.ieee.org](#)

... function will be evaluated dependent on the input **combination**. ... the circuit could be obtained from **static timing** analysis ... The partial scan of the **domino** N-block ...

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[Issues in the Design of \*\*Domino\*\* Logic Circuits - group of 5 »](#)

P Srivastava, A Pua, L Welch - Proceedings of the ACM/SIGDA Great Lakes Symposium on